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Description

Method for improving thermal process steps

The invention relates to a method for improving thermal process steps in the patterning of semiconductor wafers, in accordance with the preamble of claim 1, as disclosed in Appl. Phys. A, Vol. A46, No. 4, pp. 255-273, 1988.

The oxides produced in these process steps are used, on the one hand, as screen oxides for the well implantations and, on the other hand, as an intermediate layer for reducing mechanical stress. The oxidation steps take place in a process chamber at relatively high process temperatures, with the result that the wafers are exposed to considerable thermal loading during these process steps, in particular in the case of high heating and cooling rates. The wafers are heated up to a stabilization step at 750°C, for example at 50°C/sec, and then up to the process temperature at a heating rate of 46°C/sec in the case of AA oxidation. The cooling rate may be 50°C/sec in the upper temperature range.

What are problematic are, in particular, the RTP processes in AA oxidation, sacrificial oxidation and in GC sidewall oxidation. The integrated gate stack, in particular, reacts sensitively to high heating rates.

The thermal loading occurring in this case can lead to lateral wafer distortions which result in uncorrectable positional errors of the structure planes lying one above the other, in particular of the contact hole planer. Positional errors

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above the other, in particular of the contact hole planes. Positional errors of this type did not occur with the hitherto customary structure widths of significantly more than 0.25 mm and the wafer material used.

With technologies of 0.25 mm for large scale integrated memory components, such positional errors in the contact hole planes, which also lead to DC yield losses, are no longer acceptable and can lead to significant losses of yield or even to the total functional incapability of entire batches.

The invention is therefore based on the object of providing a method for improving thermal process steps in which the disadvantages described above are avoided.

In the case of a method of the type mentioned in the introduction, the formulation of the object on which the invention is based is achieved by virtue of the fact that the wafer is heated at a heating rate of approximately 12°C/sec up to a brief stabilization step at constant temperature and then up to the envisaged process temperature at a heating rate of 10°C/sec and, after the process time has elapsed, is cooled down to room temperature at a predetermined low cooling rate.

The stabilization step is preferably raised to a temperature of 120°C below the process temperature and is 1000°C, for example.

With the reduction of the heating rate and the shifting of the stabilization temperature from hitherto 750°C to 120°C below the process temperature, the temperature response is homogenized over the wafer. As a result, wafer distortions no longer occur.

oxidation processes, i.e. during AA oxidation, sacrificial oxidation and GC sidewall oxidation.

In a continuation of the invention, the wafer is cooled at a cooling rate of approximately 20°C/sec in the high-temperature range. This prevents wafer distortions from being able to occur during cooling.

Preferably, the wafer, at least in the temperature range in which wafer distortions can occur, is cooled at the cooling rate of approximately 20°C/sec from the process temperature to 120° below the process temperature.

Furthermore, it is advantageous if the flushing step at the start of the recipe is reduced to an extent such that the chamber is still sufficiently flushed with process gas and the cooling step at the end of the recipe is reduced to an extent such that the exit temperature is 600°C, with the overall result that the process time is reduced.

The invention will be explained in more detail below using an exemplary embodiment in connection with the figure, a temperature profile for AA oxidation being illustrated in the associated figure of the drawing.

The wafer is heated in a process chamber proceeding from room temperature R at a heating rate of 12°C/sec up to the stabilization step S, which is fixed at 120°C below the process temperature P to be reached, that is to say at 1000°C in the example. The time period of the stabilization step is a few seconds.

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Further heating to the process temperature of 1120°C us effected at a heating rate of 10°C/sec.

Raising the stabilization step to 120°C below the process temperature and reducing the heating rates has the

errors in the contact hole planes are at any rate eliminated by the method according to the invention. The consequence is a considerable improvement in the yield and a reduction of the DC yield losses by 7-10%, the outlay concerning the change of recipes of the RTP processes being very low.